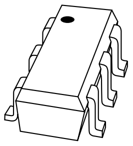


BF1205C

Dual N-channel dual gate MOS-FET

Rev. 02 — 15 August 2006 Product data sheet

1. Product profile

1.1 General description

The BF1205C is a combination of two dual gate MOS-FET amplifiers with shared source and gate 2 leads and an integrated switch. The integrated switch is operated by the gate 1 bias of amplifier b.

The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT363 micro-miniature plastic package.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Two low noise gain controlled amplifiers in a single package; one with a fully integrated bias and one with a partly integrated bias
- Internal switch to save external components
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

1.3 Applications

- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage
  - digital and analog television tuners
  - professional communication equipment.

PHILIPS

1.4 Quick reference data

Table 1. Quick reference data

Per MOS-FET unless otherwise specified.

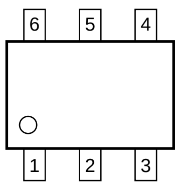
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage			-	-	6	V
I_D	drain current (DC)			-	-	30	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C	[1]	-	-	180	mW
$\lvert y_{fs} \rvert$	forward transfer admittance	f = 1 MHz					
		amplifier a; I_D = 19 mA		26	31	41	mS
		amplifier b; I_D = 13 mA		28	33	43	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1	f = 1 MHz					
		amplifier a		-	2.2	2.7	pF
		amplifier b		-	2.0	2.5	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz		-	20	-	fF
NF	noise figure	amplifier a; f = 400 MHz		-	1.3	1.9	dB
		amplifier b; f = 800 MHz		-	1.4	2.1	dB
X_{mod}	cross-modulation	input level for k = 1 % at 40 dB AGC					
		amplifier a		100	105	-	dBμV
		amplifier b		100	103	-	dBμV
T_j	junction temperature			-	-	150	°C

[1] T_{sp} is the temperature at the soldering point of the source lead.

2. Pinning information

Table 2. Discrete pinning

Pin	Description	Simplified outline	Symbol
1	gate 1 (a)		
2	gate 2		
3	gate 1 (b)		
4	drain (b)		
5	source		
6	drain (a)		



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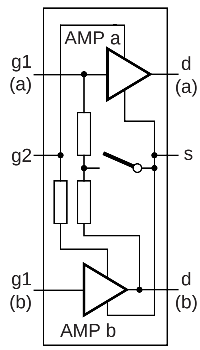


sym033

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BF1205C	-	plastic surface mounted package; 6 leads	SOT363

4. Marking

Table 4. Marking

Type number	Marking code[1]
BF1205C	M6*

[1] * = p or -: made in Hong Kong.
* = t: made in Malaysia.
* = W: made in China.

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per MOS-FET					
V_{DS}	drain-source voltage		-	6	V
I_D	drain current (DC)		-	30	mA
I_{G1}	gate 1 current		-	±10	mA
I_{G2}	gate 2 current		-	±10	mA
P_{tot}	total power dissipation	$T_{sp} \leq 107$ °C [1]	-	180	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	150	°C

[1] T_{sp} is the temperature at the soldering point of the source lead.

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-s)}$	thermal resistance from junction to soldering point		240	K/W

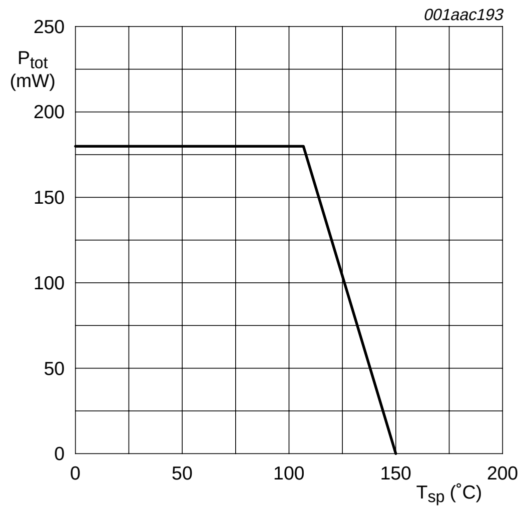


Fig 1. Power derating curve.

7. Static characteristics

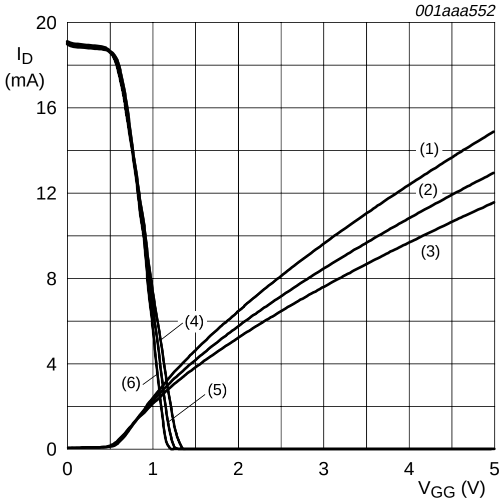
Table 7. Static characteristics

T_j = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per MOS-FET; unless otherwise specified							
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1\text{-}S} = V_{G2\text{-}S}$ = 0 V; I_D = 10 μA					
		amplifier a		6	-	-	V
		amplifier b		6	-	-	V
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{GS} = V_{DS}$ = 0 V; $I_{G1\text{-}S}$ = 10 mA		6	-	10	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{GS} = V_{DS}$ = 0 V; $I_{G2\text{-}S}$ = 10 mA		6	-	10	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S} = V_{DS}$ = 0 V; $I_{S\text{-}G1}$ = 10 mA		0.5	-	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S} = V_{DS}$ = 0 V; $I_{S\text{-}G2}$ = 10 mA		0.5	-	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 100 μA		0.3	-	1.0	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	V_{DS} = 5 V; $V_{G1\text{-}S}$ = 5 V; I_D = 100 μA		0.4	-	1.0	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; $V_{DS(b)}$ = 5 V; R_{G1} = 150 kΩ					
		amplifier a; $V_{DS(a)}$ = 5 V	[1]	14	-	24	mA
		amplifier b	[2]	9	-	17	mA
$I_{G1\text{-}S}$	gate 1 cut-off current	$V_{G2\text{-}S} = V_{DS(a)}$ = 0 V					
		amplifier a; $V_{G1\text{-}S(a)}$ = 5 V; $I_{D(b)}$ = 0 A		-	-	50	nA
		amplifier b; $V_{G1\text{-}S(b)}$ = 5 V; $V_{DS(b)}$ = 0 V		-	-	50	nA
$I_{G2\text{-}S}$	gate 2 cut-off current	$V_{G2\text{-}S}$ = 4 V; $V_{G1\text{-}S(a)} = V_{DS(a)} = V_{DS(b)}$ = 0 V; $V_{G1\text{-}S(b)}$ = 0 V;		-	-	20	nA

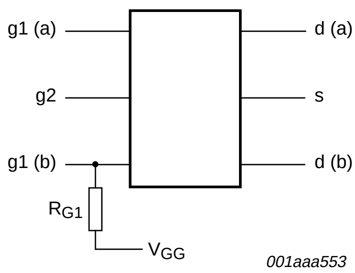
[1] R_{G1} connects gate 1 (b) to V_{GG} = 0 V (see Figure 3).

[2] R_{G1} connects gate 1 (b) to V_{GG} = 5 V (see Figure 3).



(1) $I_{D(b)}$; R_{G1} = 120 kΩ.
(2) $I_{D(b)}$; R_{G1} = 150 kΩ.
(3) $I_{D(b)}$; R_{G1} = 180 kΩ.
(4) $I_{D(a)}$; R_{G1} = 180 kΩ.
(5) $I_{D(a)}$; R_{G1} = 150 kΩ.
(6) $I_{D(a)}$; R_{G1} = 120 kΩ.

Fig 2. Drain currents of MOS-FET a and b as function of V_{GG}.



V_{GG} = 5 V: amplifier a is off; amplifier b is on
V_{GG} = 0 V: amplifier a is on; amplifier b is off.

Fig 3. Functional diagram.

8. Dynamic characteristics

8.1 Dynamic characteristics for amplifier a

Table 8. Dynamic characteristics for amplifier a[1]
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 19 mA.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\lvert y_{fs}\rvert$	forward transfer admittance	T_j = 25 °C	26	31	41	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	-	2.2	2.7	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	-	3.0	-	pF
C_{oss}	output capacitance	f = 1 MHz	-	0.9	-	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	-	20	-	fF
G_{tr}	power gain	$B_S = B_{S(opt)}$; $B_L = B_{L(opt)}$				
		f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS	31	35	39	dB
		f = 400 MHz; G_S = 2 mS; G_L = 1 mS	26	30	34	dB
		f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS	21	25	29	dB
NF	noise figure	f = 11 MHz; G_S = 20 mS; B_S = 0 S	-	3.0	-	dB
		f = 400 MHz; $Y_S = Y_{S(opt)}$	-	1.3	1.9	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$	-	1.4	2.1	dB

Table 8. Dynamic characteristics for amplifier a[1] *...continued*

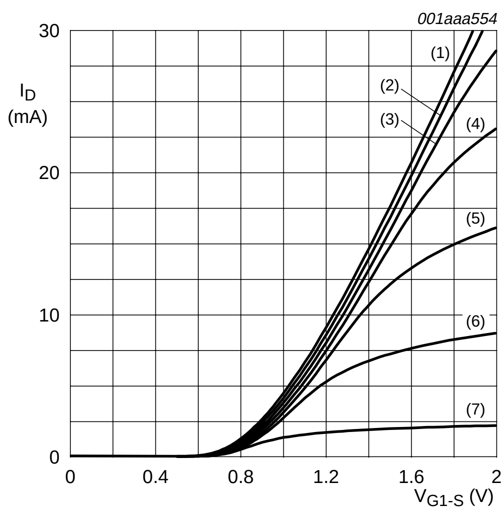
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 19 mA.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
X_{mod}	cross-modulation	input level for k = 1 %; f_w = 50 MHz; f_{unw} = 60 MHz [2]				
		at 0 dB AGC	90	-	-	dBμV
		at 10 dB AGC	-	90	-	dBμV
		at 20 dB AGC	-	99	-	dBμV
		at 40 dB AGC	100	105	-	dBμV

[1] For the MOS-FET not in use: $V_{G1-S(b)}$ = 0 V; $V_{DS(b)}$ = 0 V.

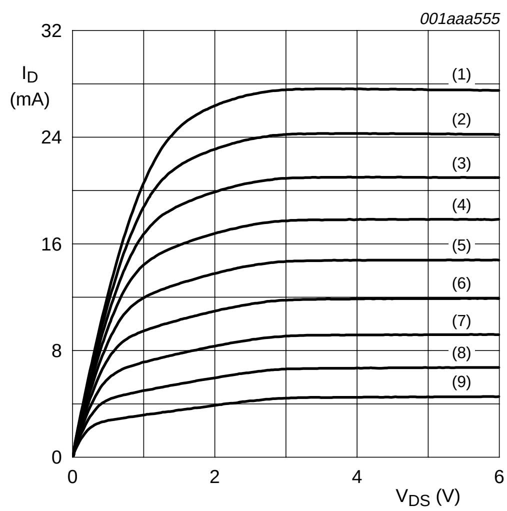
[2] Measured in Figure 33 test circuit.

8.1.1 Graphs for amplifier a



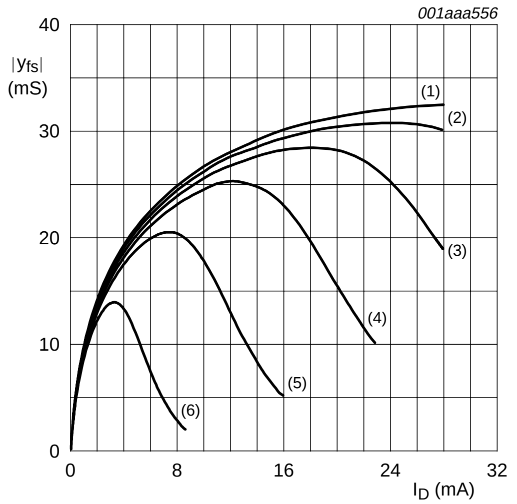
(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.
$V_{DS(a)}$ = 5 V; $V_{G1-S(b)}$ = $V_{DS(b)}$ = 0 V; T_j = 25 °C.

Fig 4. Transfer characteristics; typical values.



(1) $V_{G1-S(a)}$ = 1.8 V.
(2) $V_{G1-S(a)}$ = 1.7 V.
(3) $V_{G1-S(a)}$ = 1.6 V.
(4) $V_{G1-S(a)}$ = 1.5 V.
(5) $V_{G1-S(a)}$ = 1.4 V.
(6) $V_{G1-S(a)}$ = 1.3 V.
(7) $V_{G1-S(a)}$ = 1.2 V.
(8) $V_{G1-S(a)}$ = 1.1 V.
(9) $V_{G1-S(a)}$ = 1 V.
V_{G2-S} = 4 V; $V_{G1-S(b)}$ = $V_{DS(b)}$ = 0 V; T_j = 25 °C.

Fig 5. Output characteristics; typical values.



(1) $V_{G2\text{-}S}$ = 4 V.

(2) $V_{G2\text{-}S}$ = 3.5 V.

(3) $V_{G2\text{-}S}$ = 3 V.

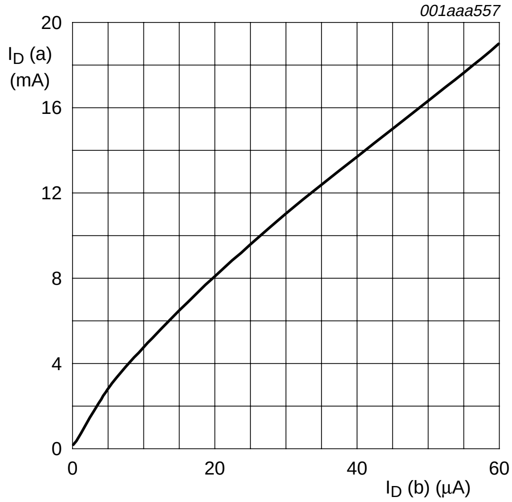
(4) $V_{G2\text{-}S}$ = 2.5 V.

(5) $V_{G2\text{-}S}$ = 2 V.

(6) $V_{G2\text{-}S}$ = 1.5 V.

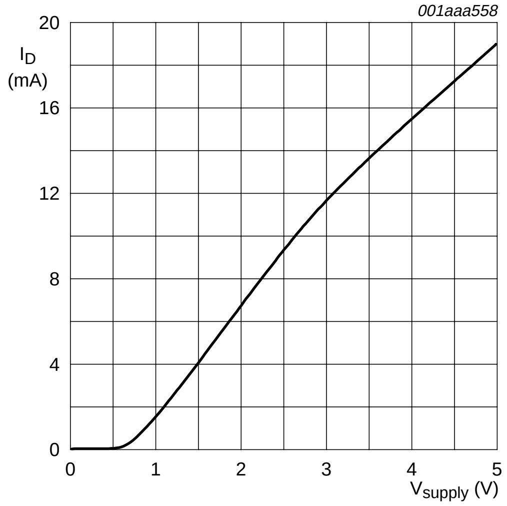
$V_{DS(a)}$ = 5 V; $V_{G1\text{-}S(b)}$ = $V_{DS(b)}$ = 0 V; T_j = 25 °C.

Fig 6. Forward transfer admittance as a function of drain current; typical values.



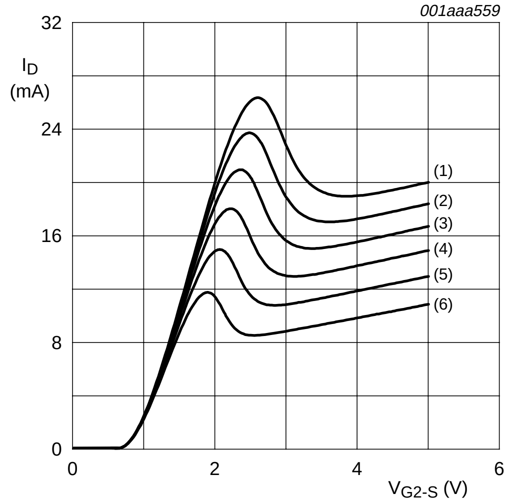
$V_{DS(a)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $V_{DS(b)}$ = 5 V; $V_{G1\text{-}S(b)}$ = 0 V; T_j = 25 °C.

Fig 7. Drain current as a function of internal G1 current (current in pin drain (b) if MOS-FET (b) is switched off); typical values.



$V_{DS(a)} = V_{DS(b)} = V_{supply}$, $V_{G2\text{-}S} = 4$ V, $T_j = 25$ °C, $R_{G1(b)} = 150$ kΩ (connected to ground); see Figure 3.

Fig 8. Drain current of amplifier a as a function of supply voltage of a and b amplifier; typical values.



(1) $V_{DS(b)} = 5$ V.

(2) $V_{DS(b)} = 4.5$ V.

(3) $V_{DS(b)} = 4$ V.

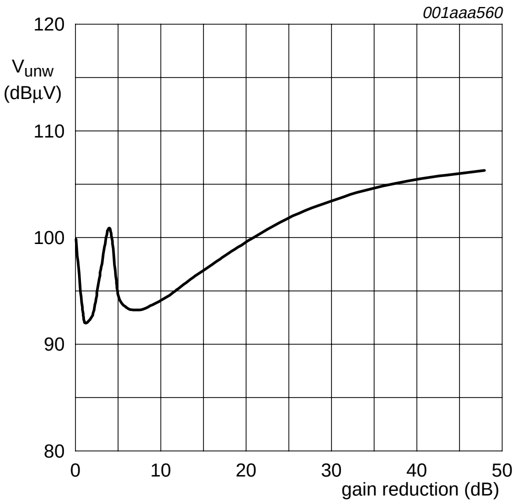
(4) $V_{DS(b)} = 3.5$ V.

(5) $V_{DS(b)} = 3$ V.

(6) $V_{DS(b)} = 2.5$ V.

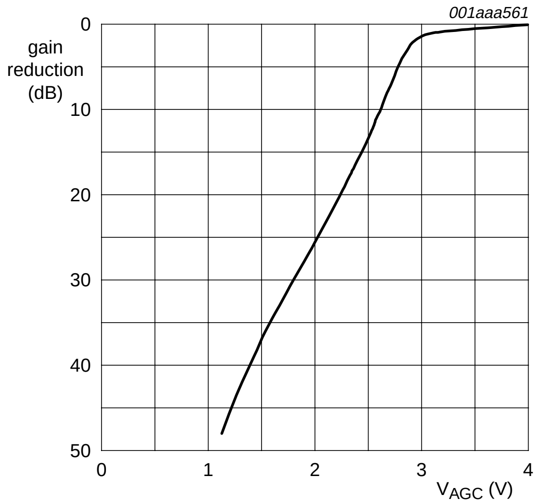
$V_{DS(a)} = 5$ V; $V_{G1\text{-}S(b)} = 0$ V; gate 1 (a) = open; $T_j = 25$ °C.

Fig 9. Drain current as a function of gate 2 and drain supply voltage; typical values.



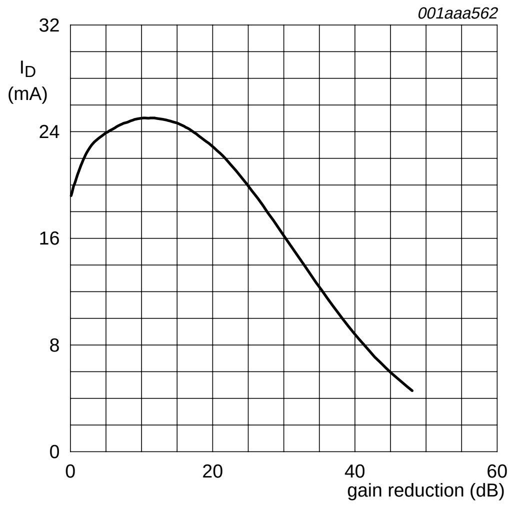
$V_{DS(a)} = V_{DS(b)} = 5$ V; $V_{G1\text{-}S(b)} = 0$ V; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; $T_{amb} = 25$ °C; see Figure 33.

Fig 10. Unwanted voltage for 1 % cross-modulation as a function of gain reduction; typical values.



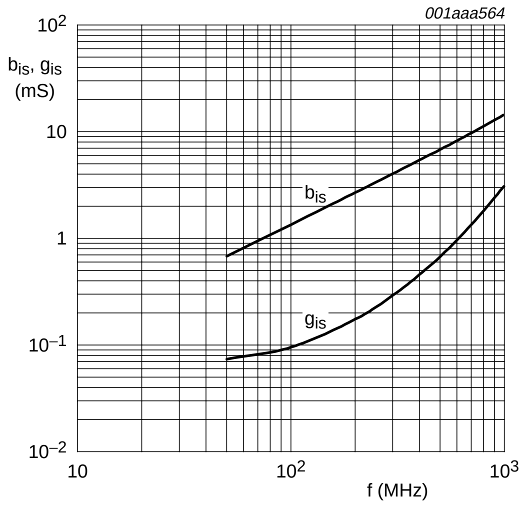
$V_{DS(a)} = V_{DS(b)} = 5$ V; $V_{G1\text{-}S(b)} = 0$ V; f = 50 MHz; see Figure 33.

Fig 11. Gain reduction as a function of AGC voltage; typical values.



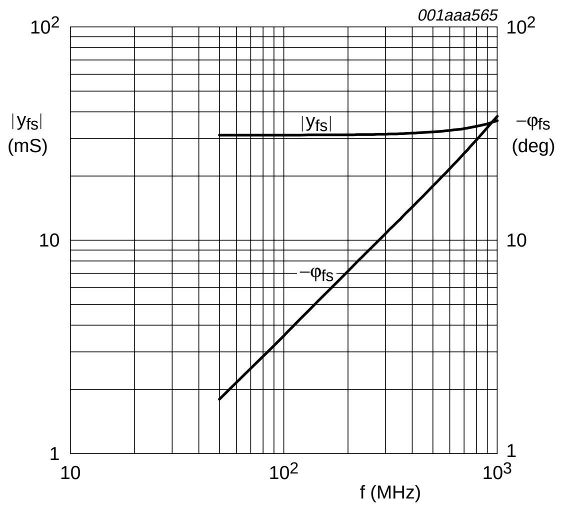
$V_{DS(a)} = V_{DS(b)} = 5$ V; $V_{G1\text{-}S(b)} = 0$ V; f = 50 MHz;
$T_{amb} = 25$ °C; see Figure 33.

Fig 12. Drain current as a function of gain reduction; typical values.



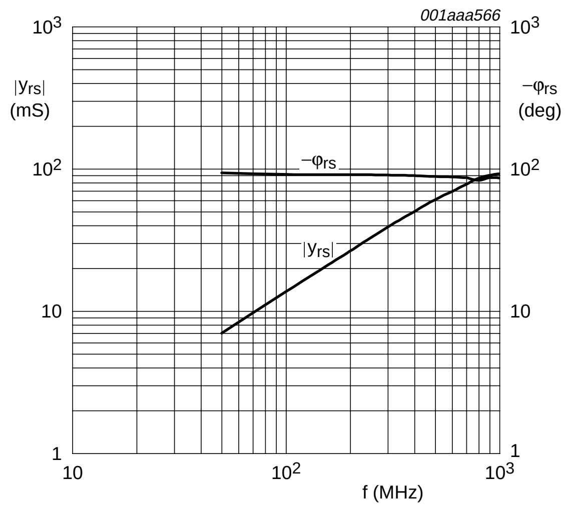
$V_{DS(a)} = 5$ V; $V_{G2\text{-}S(a)} = 4$ V; $V_{DS(b)} = V_{G1\text{-}S(b)} = 0$ V;
$I_{D(a)} = 19$ mA.

Fig 13. Input admittance as a function of frequency; typical values.



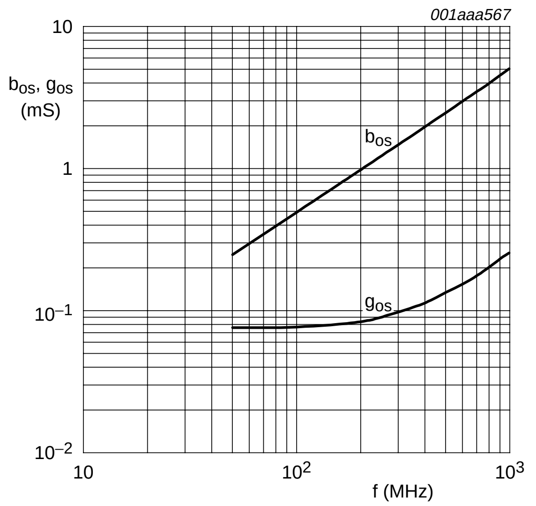
$V_{DS(a)} = 5$ V; $V_{G2\text{-}S(a)} = 4$ V; $V_{DS(b)} = V_{G1\text{-}S(b)} = 0$ V;
$I_{D(a)} = 19$ mA.

Fig 14. Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS(a)} = 5$ V; $V_{G2\text{-}S(a)} = 4$ V; $V_{DS(b)} = V_{G1\text{-}S(b)} = 0$ V;
$I_{D(a)} = 19$ mA.

Fig 15. Reverse transfer admittance and phase as a function of frequency: typical values.



$V_{DS(a)}$ = 5 V; $V_{G2\text{-}S(a)}$ = 4 V; $V_{DS(b)}$ = $V_{G1\text{-}S(b)}$ = 0 V; $I_{D(a)}$ = 19 mA.

Fig 16. Output admittance as a function of frequency; typical values.

8.1.2 Scattering parameters for amplifier a

Table 9. Scattering parameters for amplifier a

$V_{DS(a)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $I_{D(a)}$ = 19 mA; $V_{DS(b)}$ = 0 V; $V_{G\text{-}1S(b)}$ = 0 V; T_{amb} = 25 °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)
50	0.992	–3.91	3.07	175.56	0.0007	83.61	0.992	–1.47
100	0.990	–7.76	3.06	171.18	0.0017	83.19	0.992	–2.93
200	0.982	–15.42	3.04	162.42	0.0026	78.19	0.990	–5.84
300	0.971	–22.99	3.01	153.79	0.0037	73.75	0.988	–8.71
400	0.956	–30.52	2.96	145.22	0.0047	69.82	0.985	–11.59
500	0.938	–37.83	2.90	136.78	0.0055	66.12	0.982	–14.48
600	0.917	–45.14	2.83	128.46	0.0061	62.11	0.979	–17.31
700	0.893	–52.31	2.76	120.20	0.0065	58.86	0.975	–20.14
800	0.867	–59.47	2.69	111.98	0.0068	58.28	0.972	–22.98
900	0.838	–66.23	2.60	103.90	0.0067	50.64	0.968	–25.85
1000	0.807	–73.10	2.52	95.875	0.0065	47.28	0.966	–28.74

8.1.3 Noise data for amplifier a

Table 10. Noise data for amplifier a

$V_{DS(a)}$ = 5 V; $V_{G2\text{-}S}$ = 4 V; $I_{D(a)}$ = 19 mA; $V_{DS(b)}$ = 0 V; $V_{G\text{-}1S(b)}$ = 0 V; T_{amb} = 25 °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n (Ω)
		ratio	(deg)	
400	1.3	0.718	16.06	0.683
800	1.4	0.677	37.59	0.681

8.2 Dynamic characteristics for amplifier b

Table 11. Dynamic characteristics for amplifier b

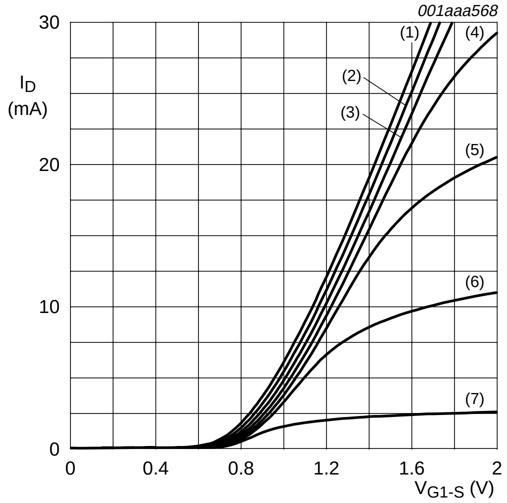
Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 13 mA.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\lvert y_{fs} \rvert$	forward transfer admittance	T_j = 25 °C		28	33	43	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz		-	2.0	2.5	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz		-	3.4	-	pF
C_{oss}	output capacitance	f = 1 MHz		-	0.85	-	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz		-	20	-	fF
G_{tr}	power gain	$B_S = B_{S(opt)}$; $B_L = B_{L(opt)}$	[1]				
		f = 200 MHz; G_S = 2 mS; G_L = 0.5 mS		31	35	39	dB
		f = 400 MHz; G_S = 2 mS; G_L = 1 mS		28	32	36	dB
		f = 800 MHz; G_S = 3.3 mS; G_L = 1 mS		24	28	32	dB
NF	noise figure	f = 11 MHz; G_S = 20 mS; B_S = 0 S		-	5	-	dB
		f = 400 MHz; $Y_S = Y_{S(opt)}$		-	1.3	1.9	dB
		f = 800 MHz; $Y_S = Y_{S(opt)}$		-	1.4	2.1	dB
X_{mod}	cross-modulation	input level for k = 1 %; f_w = 50 MHz; f_{unw} = 60 MHz	[2]				
		at 0 dB AGC		90	-	-	dBμV
		at 10 dB AGC		-	88	-	dBμV
		at 20 dB AGC		-	94	-	dBμV
		at 40 dB AGC		100	103	-	dBμV

[1] For the MOS-FET not in use: $V_{G1-S(a)}$ = 0 V; $V_{DS(a)}$ = 0 V.

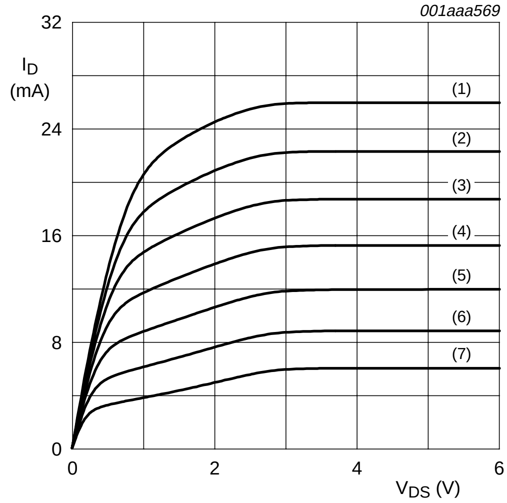
[2] Measured in Figure 34 test circuit.

8.2.1 Graphs for amplifier b



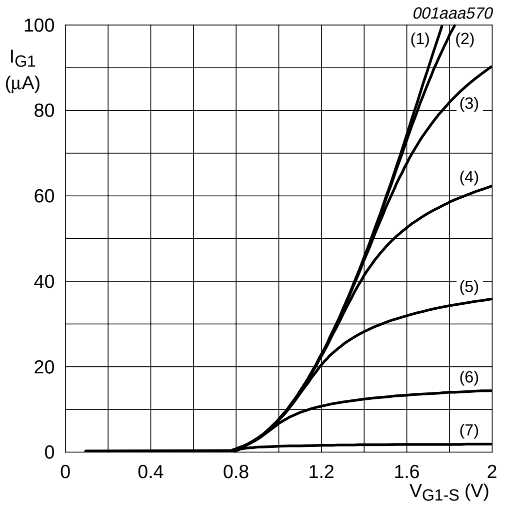
(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.
$V_{DS(b)}$ = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; T_j = 25 °C.

Fig 17. Transfer characteristics; typical values.



(1) $V_{G1-S(b)}$ = 1.6 V.
(2) $V_{G1-S(b)}$ = 1.5 V.
(3) $V_{G1-S(b)}$ = 1.4 V.
(4) $V_{G1-S(b)}$ = 1.3 V.
(5) $V_{G1-S(b)}$ = 1.2 V.
(6) $V_{G1-S(b)}$ = 1.1 V.
(7) $V_{G1-S(b)}$ = 1 V.
V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; T_j = 25 °C.

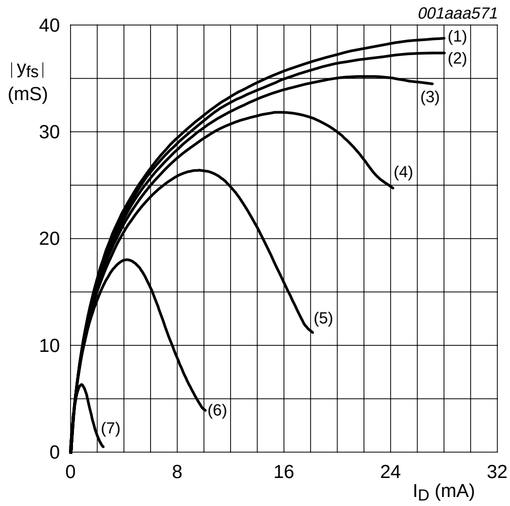
Fig 18. Output characteristics; typical values.



(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

$V_{DS(b)}$ = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; T_j = 25 °C.

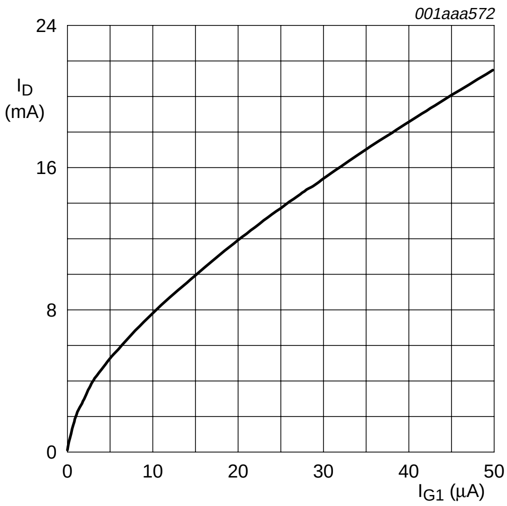
Fig 19. Gate 1 current as a function of gate 1 voltage; typical values.



(1) V_{G2-S} = 4 V.
(2) V_{G2-S} = 3.5 V.
(3) V_{G2-S} = 3 V.
(4) V_{G2-S} = 2.5 V.
(5) V_{G2-S} = 2 V.
(6) V_{G2-S} = 1.5 V.
(7) V_{G2-S} = 1 V.

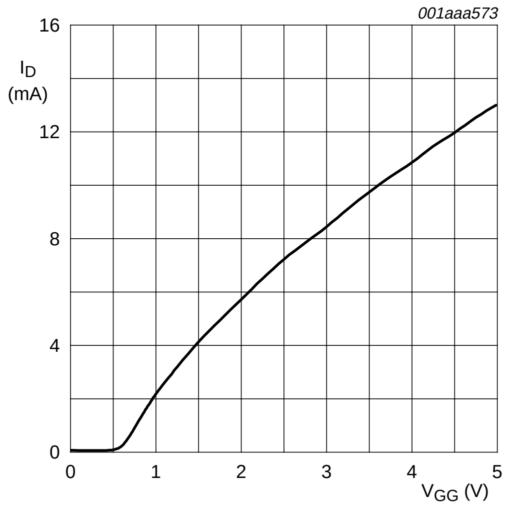
$V_{DS(b)}$ = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; T_j = 25 °C.

Fig 20. Forward transfer admittance as a function of drain current; typical values.



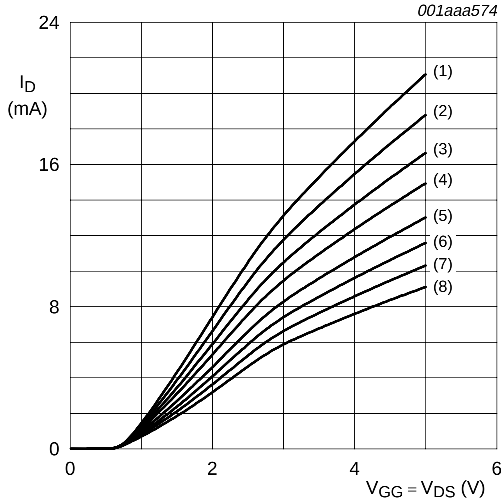
$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
T_j = 25 °C.

Fig 21. Drain current as a function of gate 1 current; typical values.



$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
T_j = 25 °C; $R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); see Figure 3.

Fig 22. Drain current as a function of gate 1 supply voltage (V_{GG}); typical values.



(1) $R_{G1(b)}$ = 68 kΩ.

(2) $R_{G1(b)}$ = 82 kΩ.

(3) $R_{G1(b)}$ = 100 kΩ.

(4) $R_{G1(b)}$ = 120 kΩ.

(5) $R_{G1(b)}$ = 150 kΩ.

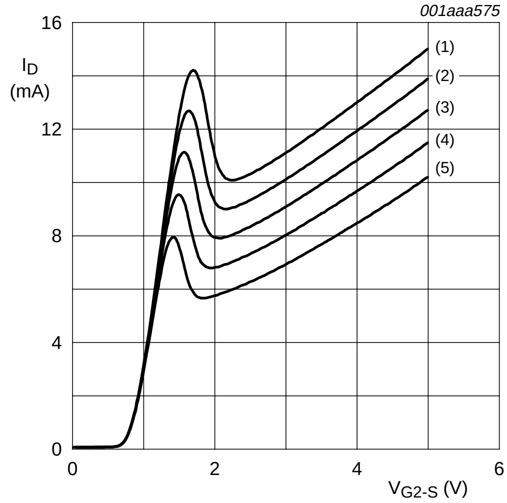
(6) $R_{G1(b)}$ = 180 kΩ.

(7) $R_{G1(b)}$ = 220 kΩ.

(8) $R_{G1(b)}$ = 270 kΩ.

V_{G2-S} = 4 V; $V_{DS(a)} = V_{G1-S(a)}$ = 0 V; T_j = 25 °C;
$R_{G1(b)}$ is connected to V_{GG}; see Figure 3.

Fig 23. Drain current as a function of gate 1 (V_{GG}), drain supply voltage and value of RG1; typical values.



(1) V_{GG} = 5.0 V.

(2) V_{GG} = 4.5 V.

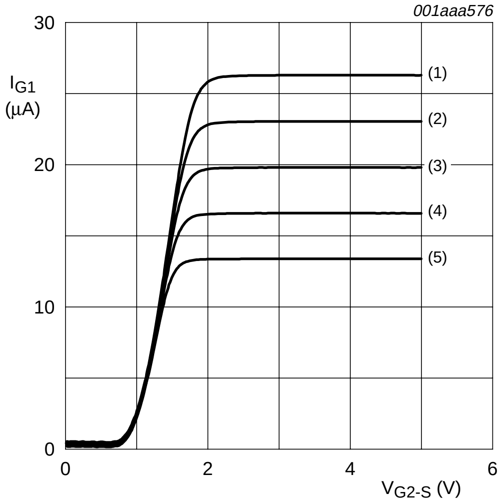
(3) V_{GG} = 4.0 V.

(4) V_{GG} = 3.5 V.

(5) V_{GG} = 3.0 V.

$V_{DS(b)}$ = 5 V; $V_{DS(a)} = V_{G1-S(a)}$ = 0 V; T_j = 25 °C;
$R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); see Figure 3.

Fig 24. Drain current as a function of gate 2 voltage; typical values.



(1) V_{GG} = 5.0 V.

(2) V_{GG} = 4.5 V.

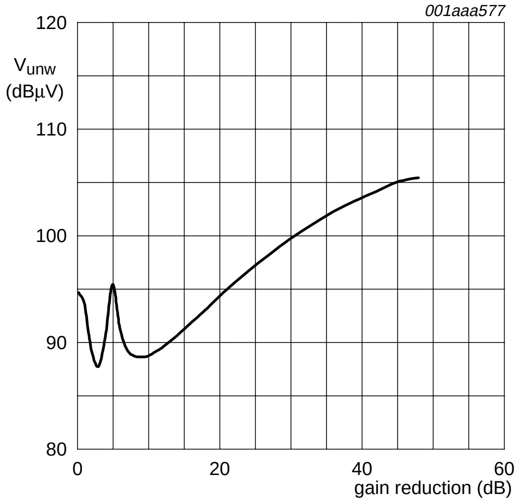
(3) V_{GG} = 4.0 V.

(4) V_{GG} = 3.5 V.

(5) V_{GG} = 3.0 V.

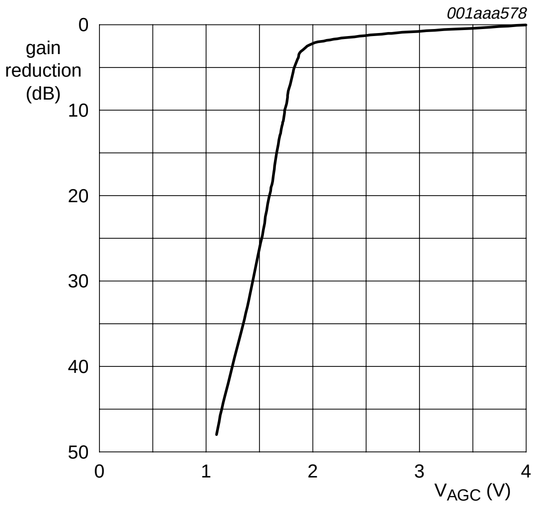
$V_{DS(b)}$ = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; T_j = 25 °C; $R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); see Figure 3.

Fig 25. Gate 1 current as a function of gate 2 voltage; typical values.



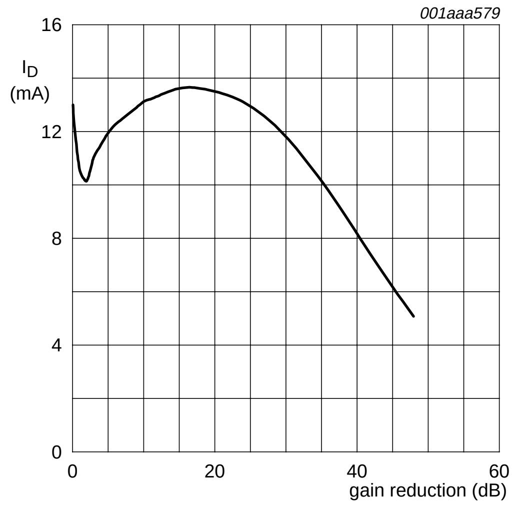
$V_{DS(b)}$ = 5 V; V_{GG} = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; $R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); f_w = 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C; see Figure 34.

Fig 26. Unwanted voltage for 1 % cross-modulation as a function of gain reduction; typical values.



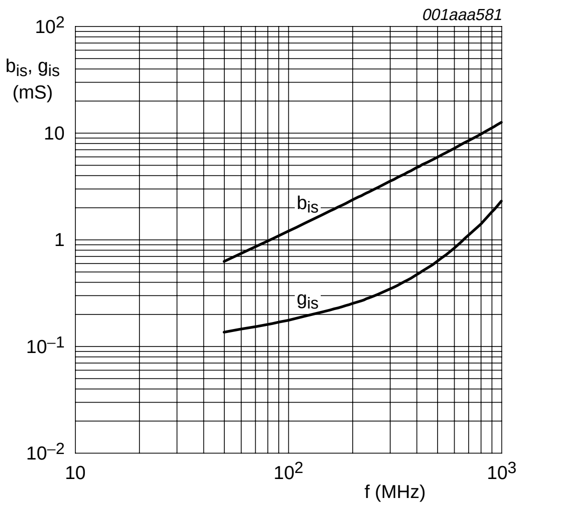
$V_{DS(b)}$ = 5 V; V_{GG} = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; $R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); f = 50 MHz; T_{amb} = 25 °C; see Figure 34.

Fig 27. Typical gain reduction as a function of AGC voltage.



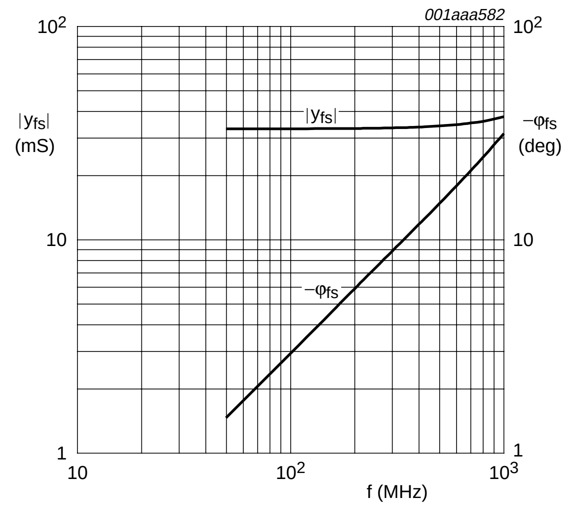
$V_{DS(b)}$ = 5 V; V_{GG} = 5 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V; $R_{G1(b)}$ = 150 kΩ (connected to V_{GG}); f = 50 MHz; T_{amb} = 25 °C; see Figure 34.

Fig 28. Drain current as a function of gain reduction; typical values.



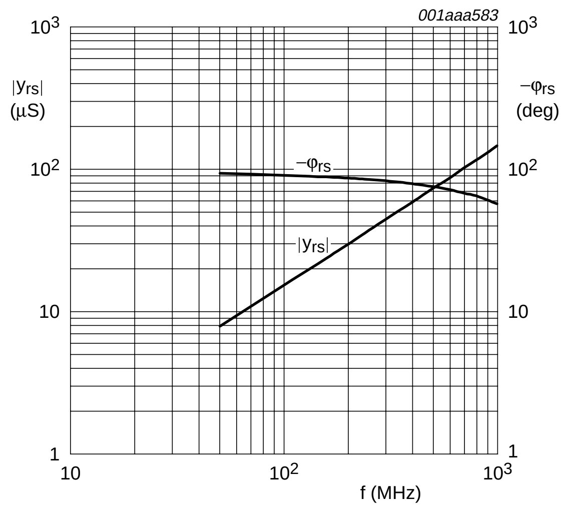
$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
$I_{D(b)}$ = 13 mA.

Fig 29. Input admittance as a function of frequency; typical values.



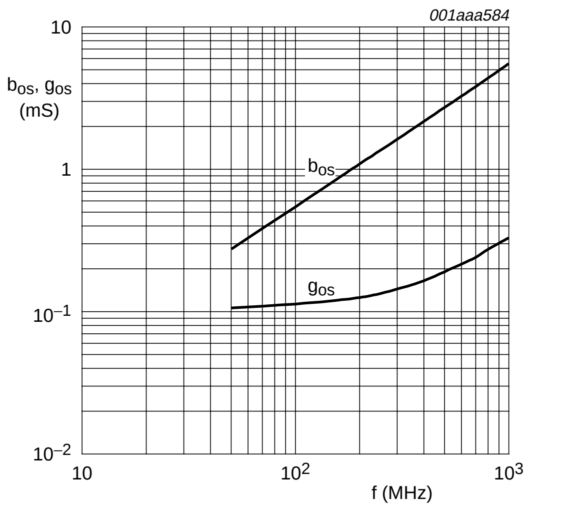
$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
$I_{D(b)}$ = 13 mA.

Fig 30. Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
$I_{D(b)}$ = 13 mA.

Fig 31. Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS(b)}$ = 5 V; V_{G2-S} = 4 V; $V_{DS(a)}$ = $V_{G1-S(a)}$ = 0 V;
$I_{D(b)}$ = 13 mA.

Fig 32. Output admittance as a function of frequency; typical values.

8.2.2 Scattering parameters for amplifier b

Table 12. Scattering parameters for amplifier b

$V_{DS(b)} = 5$ V; $V_{G2\text{-}S} = 4$ V; $I_{D(b)} = 13$ mA; $V_{DS(a)} = 0$ V; $V_{G1\text{-}S(a)} = 0$ V; $T_{amb} = 25$ °C.

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)	Magnitude ratio	Angle (deg)
50	0.986	–3.66	3.26	175.93	0.0008	84.23	0.988	–1.65
100	0.982	–7.01	3.24	172.04	0.0015	84.91	0.988	–3.27
200	0.975	–13.71	3.22	164.24	0.0029	83.96	0.986	–6.50
300	0.966	–20.36	3.19	156.53	0.0042	82.86	0.984	–9.69
400	0.955	–27.04	3.15	148.86	0.0055	81.88	0.982	–12.88
500	0.943	–33.62	3.10	141.24	0.0066	80.92	0.978	–16.07
600	0.927	–40.16	3.05	133.70	0.0076	80.15	0.975	–19.21
700	0.909	–46.70	2.99	126.13	0.0086	79.68	0.972	–22.35
800	0.891	–52.07	2.92	118.64	0.0094	78.28	0.968	–25.52
900	0.868	–59.48	2.84	111.09	0.0100	78.28	0.965	–28.65
1000	0.846	–65.86	2.77	103.58	0.0107	78.15	0.961	–31.85

8.2.3 Noise data for amplifier b

Table 13. Noise data for amplifier b

$V_{DS(b)} = 5$ V; $V_{G2\text{-}S} = 4$ V; $I_{D(b)} = 13$ mA; $V_{DS(a)} = 0$ V; $V_{G1\text{-}S(a)} = 0$ V; $T_{amb} = 25$ °C.

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n (Ω)
		ratio	(deg)	
400	1.3	0.695	13.11	0.694
800	1.4	0.674	32.77	0.674

9. Test information

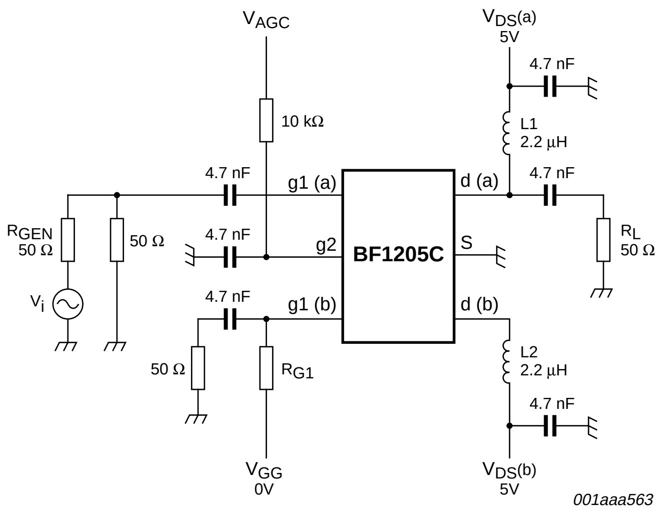


Fig 33. Cross-modulation test set-up for amplifier a.

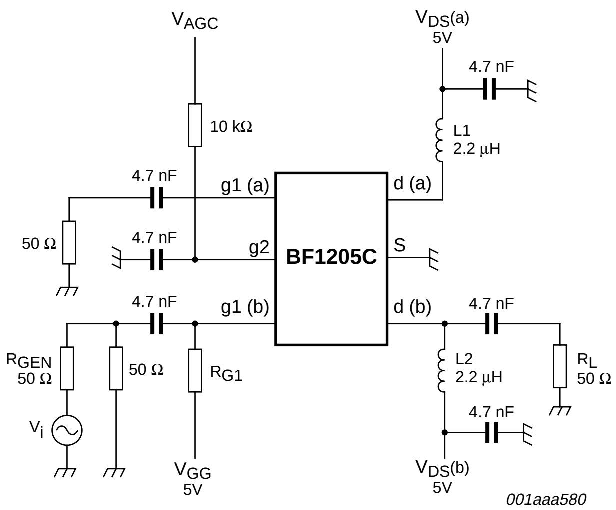
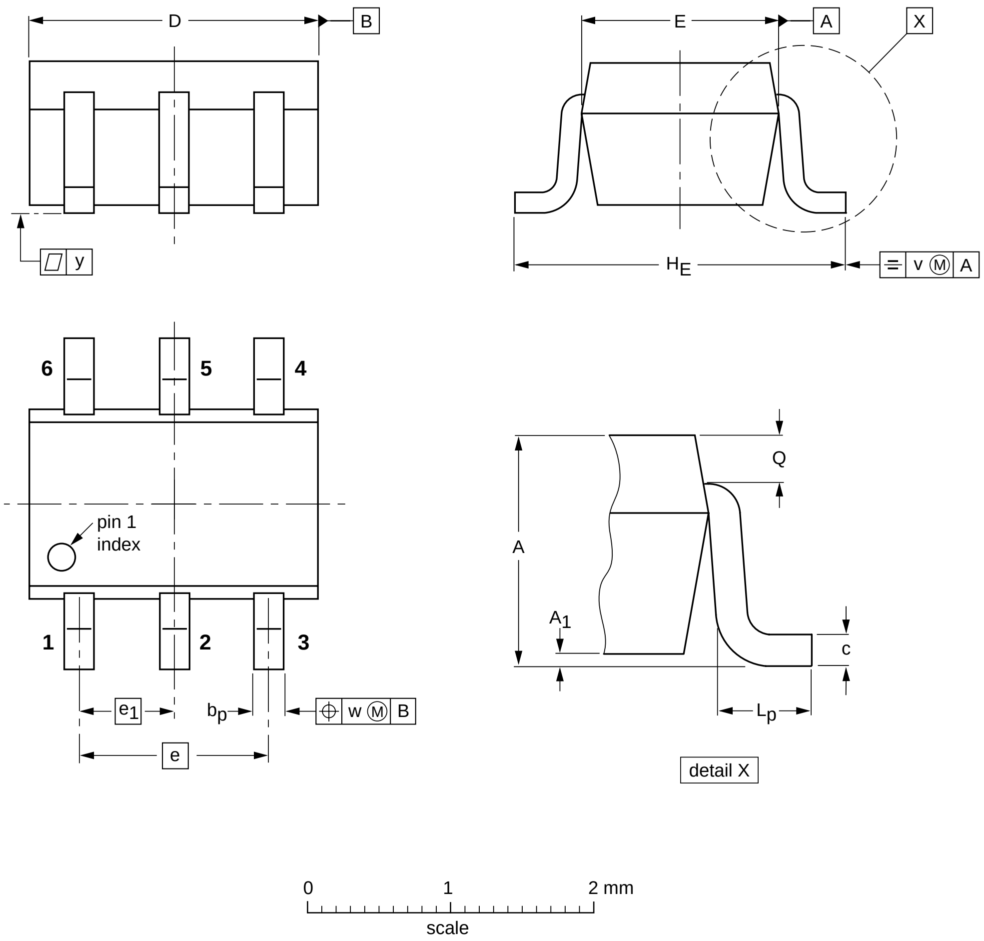


Fig 34. Cross-modulation test set-up for amplifier b.

10. Package outline

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

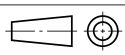
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

Fig 35. Package outline.

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1205C_2	20060815	Product data sheet	-	BF1205C_1 (9397 750 13005)
Modifications:	• Figure 1: replaced drawing with correct drawing 001aac193			
BF1205C_1 (9397 750 13005)	20040518	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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14. Contents

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